

Abstract

The invention proposes an improved twin MONOS memory device and its fabrication. The ONO layer is self-aligned to the control gate horizontally. The vertical insulator between the control gate and the word gate does not include a nitride layer. This prevents the problem of electron trapping. The device can be fabricated to pull the electrons out through either the top or the bottom oxide layer of the ONO insulator. The device also incorporates a raised memory bit diffusion between the control gates to reduce bit resistance. The twin MONOS memory array can be embedded into a standard CMOS circuit by the process of the present invention.